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Channel Engineering for Submicron N-Channel MOSFET Based on TCAD Simulation

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Abstract: This paper discusses the optimization of 0.8 micron physical gate N-channel MOSFET devices focusing on channel engineering. Based on the semiconductor process simulation sentaurus process and the device simulation sentaurus devices, In this study, we characterize the effect of the channel modulation by engineering doping concentration profile, gate oxide thickness, and determine how to enhance the performance of N-channel MOSFET. Our simulation show that, the effect of channel engineering on the basis electrical characteristics such as threshold voltage in linear and saturation region, subthreshold swing, off state drain leakage current, saturation drain current and also the Drain Induced Barrier Lowering (DIBL) of N-channel MOSFET in 0.8 µm CMOS technology fabrication of Thai Micro Electronics Center (TMEC). Finally, the effect of channel engineering of N-channel MOSFET is discussed.

Key words: MOSFET, DIBL, CMOS, Channel engineering.

INTRODUCTION

As MOSFET scaling continues, not only ultra-shallow junction but also channel profile optimization are essential for device performance improvement and short channel effect (SCE) control. The onset of short channel effects, such as drain-induced barrier lowering, punchthrough, and shifts in threshold voltage (dV_{TH}), severely affect MOS device performance. To control punchthrough, conventional MOSFET's must have progressively higher doping in the channel region as the gate length is decreased. High channel doping makes it difficult to control and is expected to result in reduced channel mobility (G. Guegan *et al,* 2001). In an attempt to overcome these limitations, channel-engineered structures have been proposed and fabricated for 0.8µm CMOS twin well technology. These devices have channel lengths as small as 0.5 µm and utilize a low doped region at the oxide interface that varies to a high doping level over depths of 40–100 nm in the channel. These theoretical studies were only based on simulation. In this paper, we propose an experimental and extensive evaluation of three channel profiles implanted in a 0.8 µm N channel MOSFET core process with a relatively thick gate oxide (15 nm). The investigation is based upon the following criteria:

- SCE control and sub-threshold slope
- Drive currents
- Off leakage currents
- Gate length and process sensitivity

The subthreshold current between the drain and source occurs in a MOS transistor when the gate voltage is below V_{TH} There are several factors which impact threshold voltage and subthreshold current. They include drain-induced barrier lowing (DIBL) effect, body effect, channel width, short channel effect and temperature effects. Mathematically, subthreshold leakage current (BSIM) can be modeled as

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$$I_{sub} = I_o \exp\left(\frac{V_{GS} - V_{TH} - \gamma V_{SB} + \eta V_{DS}}{n(v_T)}\right)\left(1 - \exp\left(\frac{-V_{DS}}{v_T}\right)\right) \quad (1)$$

$$I_o = \mu_o C_{ox} \frac{W}{L_{eff}} (v_T)^2 \exp(1.8) \quad (2)$$

Where μ_0 is the zero bias mobility, C_{ox} is the gate oxide capacitance, W and L_{eff} are transistor width and effective channel length, v_T is the thermal voltage given by (kT / q), V_{TH} is the threshold voltage, g is the body effect coefficient, V_{SB} is the source body voltage bias, V_{DS} is drain supply voltage, η is the DIBL coefficient, q is the electron charge, and n is the transistor subthreshold swing coefficient . And off state leakage current (I_{off}) is defined by the subthreshold current at 0V of V_{GS} and 5V of V_{DS}. Then the term $(1 - \exp(-V_{DS} / v_T))$ can be neglected. Then the off state leakage current can be described as following.

$$I_{off} = I_o \exp\left(\frac{-V_{TH} - \gamma V_{SB} + \eta V_{DS}}{n(v_T)}\right) \quad (3)$$

It can be seen that a channel length increase will not only directly reduce I_{off}, but also increase V_{TH}, which further reduces I_{off}.

MATERIALS AND METHODS

For this study, the p-well was from by boron implantation on p type substrate 20 ohm-cm. A self align n+ polysilicon gate 350 nm of thickness was used with gate oxide 15 nm of thickness. A BF_2^+ ion implantation for threshold voltage adjusts in a channel was implemented in order to match the threshold voltage of the NMOS and PMOS device, as require in the modern CMOS technology process shown in Fig.1. A spacer technology (spacer width of 200nm) with heavily doped source/drain extensions is used. The source/drain

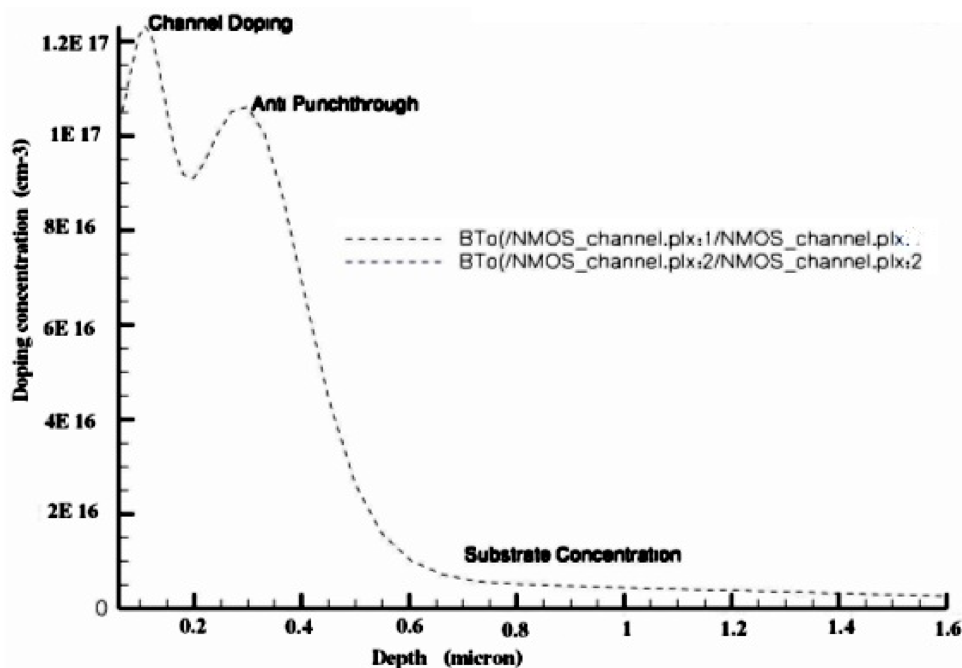

Fig. 1: Doping concentration profile versus depth in substrate.

extensions and deep source/drain junction depths are 20nm and 500 nm respectively. Simulations are performed for channel lengths of L = 0.5, 0.6, 0.7, 0.8, 1.0 and 3.0 µm. Figure.2 show the simulated NMOS structure with design gate length of 0.5 micron. All device simulations are performed using sentaurus devices 2-D. The models activated in simulation include the carrier mobility degradations due to high doping concentration, the velocity saturation within high-field regions and the mobility degradation due to surface roughness scattering.

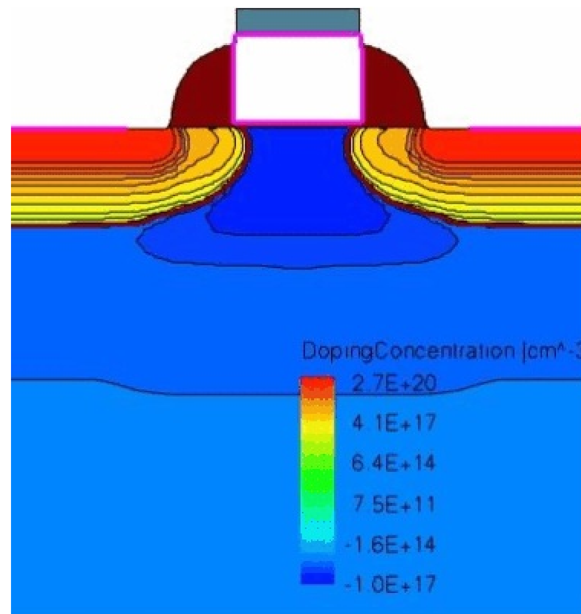

Fig. 2: The simulated NMOS structure of L=0.5 µm.

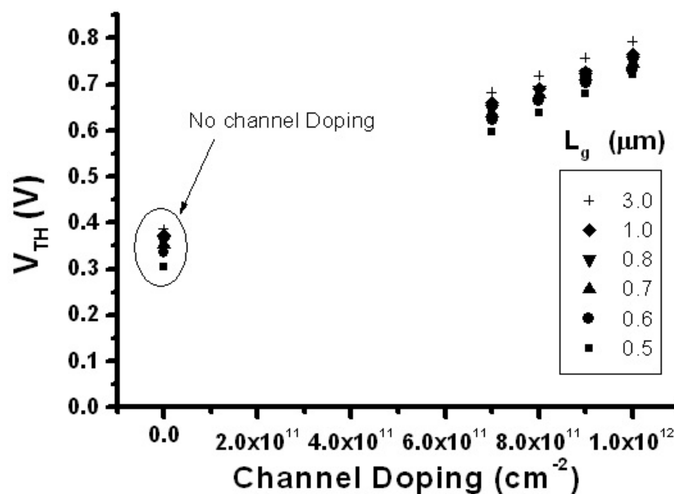

Fig. 3: V_{TH} versus channel doping with *Lg* as a parameter.

RESULTS AND DISCUSSION

To carry out this channel engineering , NMOSFETs with physical design gate lengths down to 0.5 µm were characterized. Fig. 3 shows the threshold voltage (V_{TH}) versus channel doping concentration profiles with various design gate length (Lg). Fig. 4 shows the threshold voltage (V_{TH}) versus design gate length (Lg) with various channel doping concentration profiles.

The threshold voltage is linearly depended on the channel doping concentration. And we observe a better control of the roll off as the design gate length is not less than 0.6 micron with all various channels doping

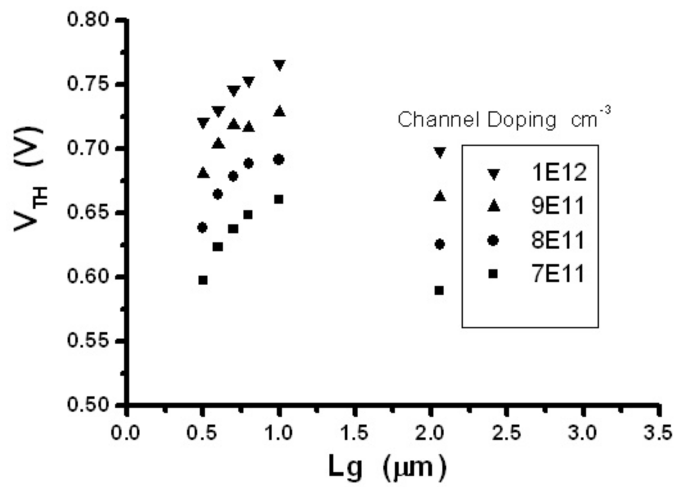

Fig. 4: V_{TH} versus *Lg* with channel doping as a parameter.

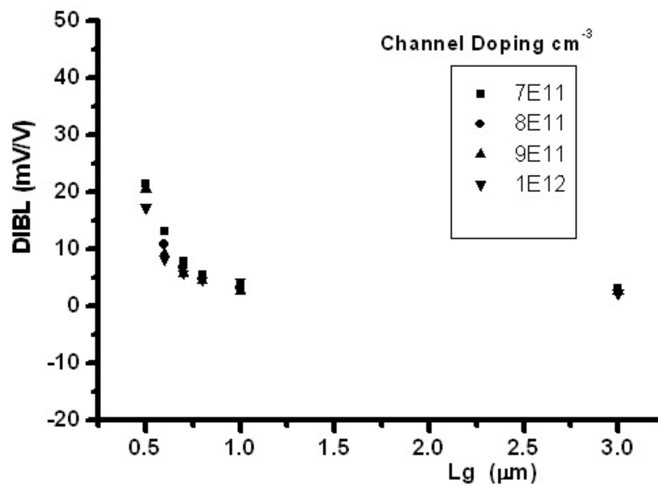

Fig. 5: DIBL versus *Lg* with various channel doping.

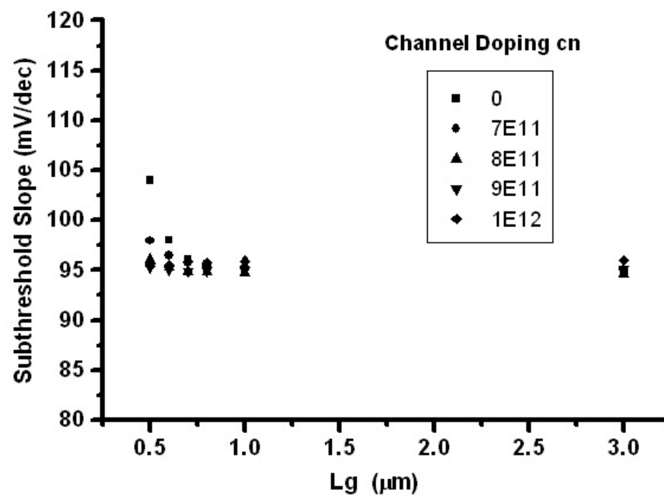

Fig. 6: Subthreshold slope versus *Lg* with various channel doping.

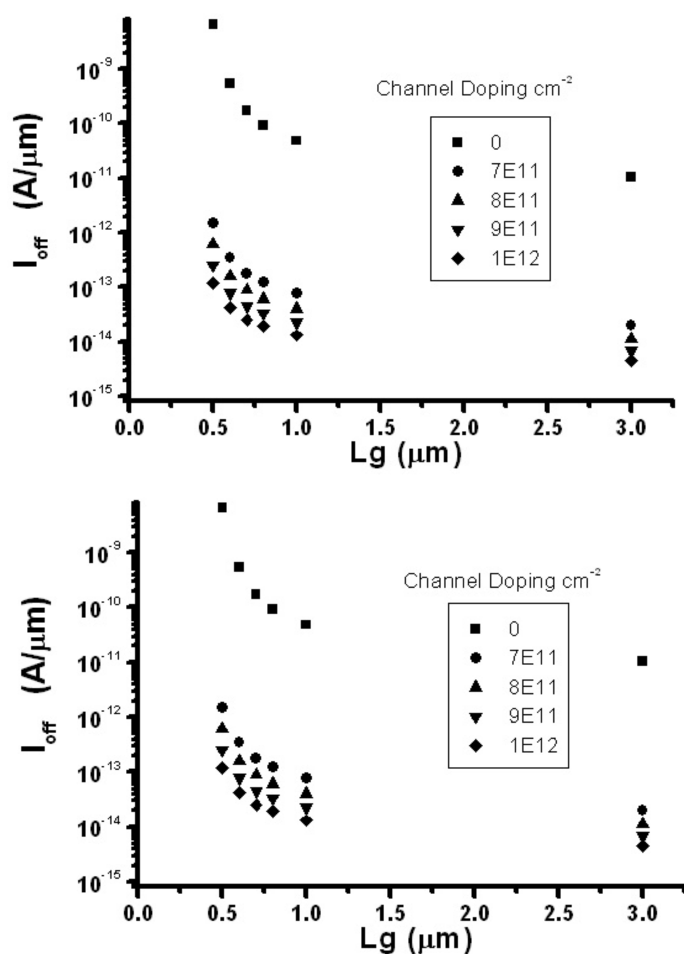

Fig. 7: I_{off} versus Lg with channel doping as a parameter.

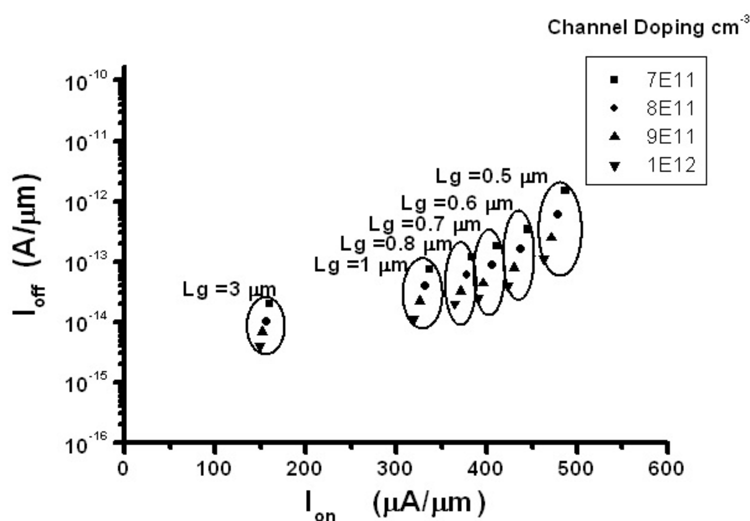

Fig. 8: I_{off} versus I_{on}. with various of Lg and channel doping concentration at fixed T_{ox} = 15nm, V_{DS} = 5 V.

concentration. The DIBL and the subthreshold slope dependence versus gate length which are plotted on Fig. 6 and 7, confirm these behaviors. There is no significant increase of the subthreshold slope at V_{DS} = 0.1 volt for NMOSFETs defined with various channels doping concentration. Fig. 7 shows I_{off} versus Lg measured

at 5.0V for the transistors with various values of channel doping concentration**.** For *Lg* < 0.6μm, the off state leakage current becomes significant part. Fig. 8 shows I_{on} versus I_{off} performances with various Lg and channel doping concentration. The minimum mask gate length should not be less than 0.6 μm due to better roll-off control.

Conclusion:

Channel profile engineering optimizations have been performed for 0.8 μm CMOS technology. The short channel effect control with relatively thick gate oxide (15 nm) is one of the main issues of the gate length scaling. Therefore, we have investigated the n channel MOSFETs performance with a various channel doping profiles on a manufacturable 0.8 μm gate length. A simulation reveal that, the channel engineering improved the threshold voltage and the off leakage current but have not a dominant effect on DIBL and subthreshold slope. In design process flow, the minimum design gate length should not be less than 0.6 mm due to V_{TH} roll-off and I_{off}-I_{on} characteristics. In conclusion, the channel engineering architecture, the expected performance of NMOSFETs with design gate length of 0.8 μm is 360 μA/mm on current.

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