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Substrate Bias Effects on Drain Induced Barrier Lowering (DIBL) in Short Channel NMOS FETs

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Abstract: The substrate biasing characteristics of the Drain-Induced Barrier Lowering (DIBL) effects in short-channel NMOS devices with n+ polysilicon gate that fabricated at TMEC by 0.8 CMOS technology were presented. It was found that by increasing the substrate bias form -1 to -5V, DIBL in NMOS devices with mask channel length (*L*) from 0.6 to 3.0 micron shows the interesting feature. As the channel length decreased, the threshold voltage shift caused by DIBL first increased with increasing substrate bias and then decreased as the channel length decreased further for the range of $L \leq$ 0.6 micron. But the DIBL increased with increasing substrate bias for the length of *L* between 0.8 and 1.2 micron. And almost neglected the substrate bias effect for the range of $L >$ 1.2 micron. The substrate bias effect on subthreshold DIBL coefficient (*ETAb*) is approximately 3.5, 7.0, 8.0 and 0.7 mV/V for *L* of 0.8, 1.0, 1.2 and 3.0 micron respectively. Whereas the subthreshold DIBL coefficient (*ETA0*)is around 44, 10, 5 and 1.25 mV/V respectively. This change in DIBL with substrate bias for a short channel device can be explained as the transition of the surface DIBL effect to the subsurface DIBL effect and the onset of the punchthrough effect. Design considerations of the channel doping profile in short channel NMOS device for substrate bias based on improving the punchthrough and DIBL are also briefly discussed.

Key words: DIBL, CMOS, NMOS

INTRODUCTION

The drain-induced barrier lowering effect is one of the most important effects in short channel MOSFET devices. The barrier lowering effect is observed by a shift of threshold voltage as a function of drain voltage of short channel devices. In short channel MOSFET, it is well known that the depletion width at source and drain junction become comparable to the channel length resulting in significant field penetration from drain to source. The potential barrier at the source is lowered due to this field penetration. The degree of the field penetration depends on the channel length, channel doping density, and oxide thickness. In addition, it depends on the junction depth of the source and drain, drain to source bias, and on source to substrate bias. The effect of decreasing channel length causes the depletion region width surround the source and drain diffusion to approach each other. Depending on the drain bias, the electric field at the drain can penetrate to the source region of the device causing a decrease in potential barrier at source. As a result, the device can conduct significant drain current due to an increase in carriers injected from the source. This mechanism is responsible for the strong dependence of subthreshold current on the drain bias. Moreover, the subthreshold current will change the threshold voltage as the drain bias is varied. In this paper, δV_{TH} (DIBL) varied linearly with the drain voltage. The effect of drain induced barrier lowering (DIBL) base on BSIM3 model in the threshold voltage was described by the following expression

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$$\delta V_{TH} = \Theta_{DIBL}\left(ETA0 + ETAbV_{BS}\right)V_{DS} \tag{1}$$

Note how the composite DIBL parameter in (1)

$$\eta = ETA0 + ETAbV_{BS} \tag{2}$$

$$\Theta_{DIBL} = \exp\left(\frac{DSUBL_{eff}}{2L_{t,DIBL}}\right) + 2\exp\left(\frac{DSUBL_{eff}}{L_{t,DIBL}}\right) \tag{3}$$

$$L_{t,DIBL} = \sqrt{\frac{\varepsilon_{si}T_{ox}}{\varepsilon_{ox}}X_d} \tag{4}$$

$$X_d = \sqrt{\frac{2\varepsilon_{si}(\Phi_s - V_{bs})}{qN_{ch}}} \tag{5}$$

Where *ETA0* is the drain induced barrier term, *ETAb* is the subthreshold DIBL coefficient, DSUB is the substrate bias effect on subthreshold DIBL coefficient, η is substrate bias effect on DIBL, η is also a composite DIBL parameter, $L_{t,DIBL}$ is the characteristics length, X_d is the depth of the gate induced depletion region in the substrate, T_{ax} is the gate oxide thickness, q is the electron charge, N_{ch} is the channel doping concentration, Φ_s is the surface potential, ε_{si} and ε_{ox} are the permittivity of silicon and silicon dioxide respectively. Includes substrate bias dependence in a form identical to that found in the second generation model. Also note that, the change in threshold voltage due to DIBL is taken to be linearly propotional to the drain bias. The purpose of this paper is to present the substrate bias characteristics of the DIBL effect versus channel length for surface channel NMOS devices.

MATERIALS AND METHODS

The NMOS test device in this paper were fabricated by 0.8 CMOS technology from Thai Micro Electronics Center (TMEC). Starting with p-type substrate of 5 ohm-cm resistance. The doping concentration of n-well was approximately $3x10^{16}$ cm^{-3} .The p-well was form by boron ion implantation with a doping concentration approximately $1x10^{16}$ cm^{-3}. A self align n+ polysilicon gate process 350 nm of thickness was used with gate oxide 25 nm of thickness. A boron ion implantation for threshold voltage adjust in a channel was implemented in order to match the threshold voltage of the NMOS and PMOS device, as require in the modern CMOS technology process. The source and drain junction depth were approximately 0.3 micron with approximately 75 ohm/square of sheet resistance. The test device had effective channel length (L_{eff}) varying from 0.4 to 2.8 micron (lateral diffusion = 0.1 micron /side) with fixed a channel width of 40 micron. The effective channel length were extracted from the maximum slope of I_{DS} - V_{GS} curves in the linear region on L-array of these MOS devices. The effective channel length is extracted by plotting inverse of maximum slope versus the mask length. The threshold voltage measurement for testing device were perform by measuring a set of log I_{DS} versus V_{GS} with drain bias voltage of 1 to 5 V (1V/step), and substrate bias voltage of 0 to -5V(1V/step) were made for these test NMOS devices using a semiconductor parameter analyzer HP4156B, with a PC personal computer as the central controller. The measurement accuracy is 0.02% for voltage and 0.06% for current within the measurement range. Fig.1 show our measurement results for the test NMOS devices with mask gate length L= 0.6, 0.8, 1.0 and 1.2 micron respectively. The gate voltage at which the drain current becomes $1x10^{-8}$A is claim the threshold voltage. The DIBL parameter is defined as the change in the threshold voltage shift δV_{TH} (DIBL) divided by the change in the drain voltage bias d V_{DS}

$$DIBL = -\frac{\delta V_{TH}}{\delta V_{DS}} = -\frac{V_{TH}(V_{DS2}) - V_{TH1}(V_{DS1})}{V_{DS2} - V_{DS1}} \tag{6}$$

In (6), V_{DSI} and V_{DS2} are chosen as 1 and 5V respectively, for all the NMOS test devices, the only exception being V_{DS2} = 2 V for the short channel NMOS devices with L=0.6 micron due to the punchthrough effect as shown in Fig. 1(d).

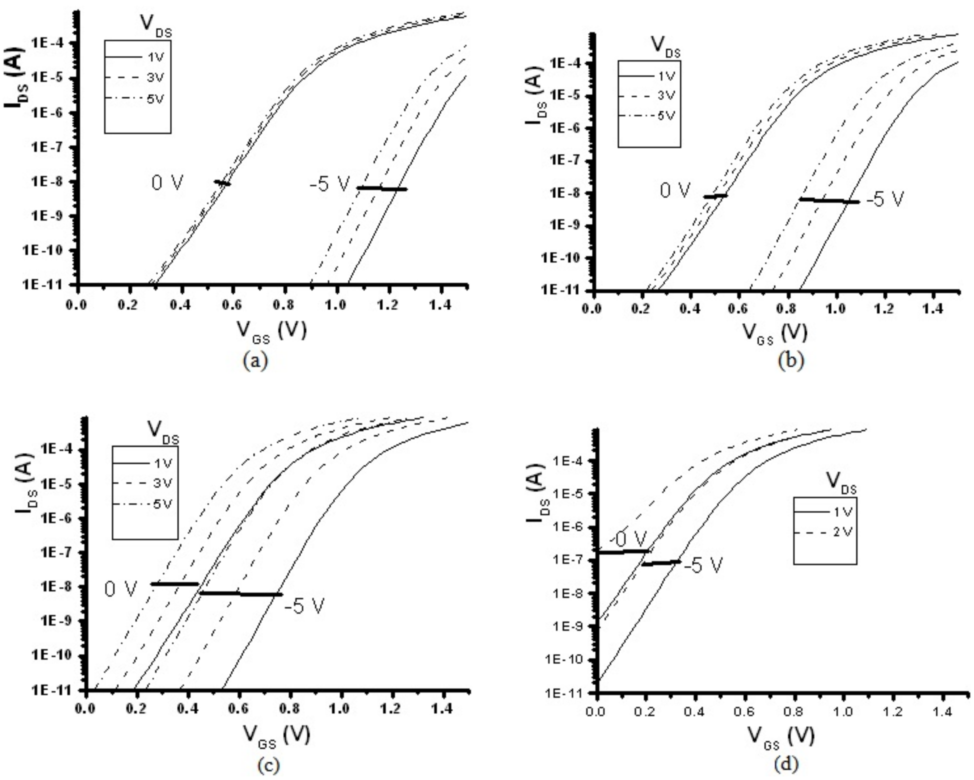

Fig. 1: Experimental curves of the drain current versus gate voltage for the test NMOS devices of (a)L=1.2 micron, W=40 micron, with V_{DS} = 1, 3 and 5V at the fixed value of substrate bias V_{BS} = 0, and -5V (b) L=1.0 micron, W=40 micron, with V_{DS} =1, 3 and 5V at the fixed value of substrate bias V_{BS} = 0, and -5V (c) L= 0.8 micron, W=40 micron, with V_{DS} = 1, 3 and 5V at the fixed value of substrate bias V_{BS} = 0, and -5V and (d) L= 0.6 micron, W=40 micron, with V_{DS} = 1 and 2V at the fixed value of substrate bias V_{BS} = 0, and -5V respectively.

RESULTS AND DISCUSSIONS

Results:

The DIBL effect of short channel NMOS devices can be determined physically as due to the field penetration from drain to source, due to the closeness of their depletion junction region. When the magnitude of the substrate bias is increased in any of testing devices, there is an overall increase in the source to channel potential barrier. In general this increase in the barrier height results in further decrease in the subthreshold current. But with an increased substrate bias the source and rain depletion layer widths also increase, which in turn result in an increased field penetration from the drain to the source. As a result the threshold voltage is reduction with respect to V_{DS} increase when the substrate bias is increased as shown in Fig.2. From the experimental results shown in Fig.1, the two main feature of the DIBL effect can be clearly seen. First, the threshold voltage shift δV_{TH} (DIBL) is almost linearly with the applied drain voltage within the measurement range of 1 to 5 V. This results was described by the following expression

$$\delta V_{TH}(DIBL) = -DIBL\delta V_{DS} \tag{7}$$

Where DIBL is also proportional to the channel length L. Second, the DIBL effect is also related to the substrate voltage bias V_{BS}. As the V_{BS} is increase, the threshold voltage and the threshold voltage shift caused by DIBL is increased for L=0.8 1.0, 1.2 micron, but is decreased for L= 0.6 micron. The DIBL effect versus channel length with different substrate voltage bias is shown in Fig. 3.

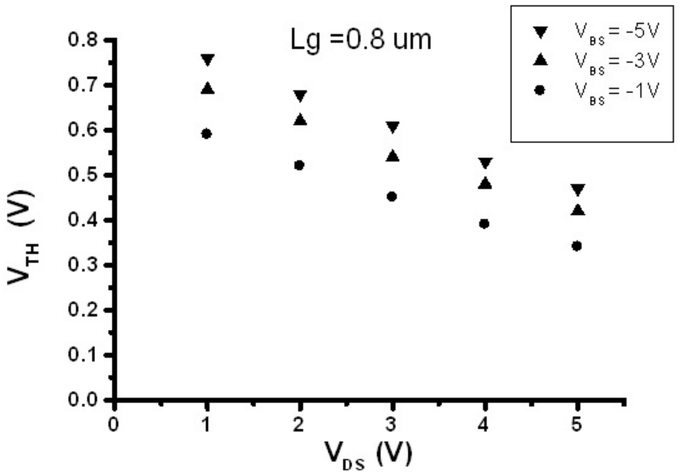

Fig. 2: The measured results of V_{TH} versus V_{DS} for NMOS devices with V_{BS} varying from -1 to -5 V.

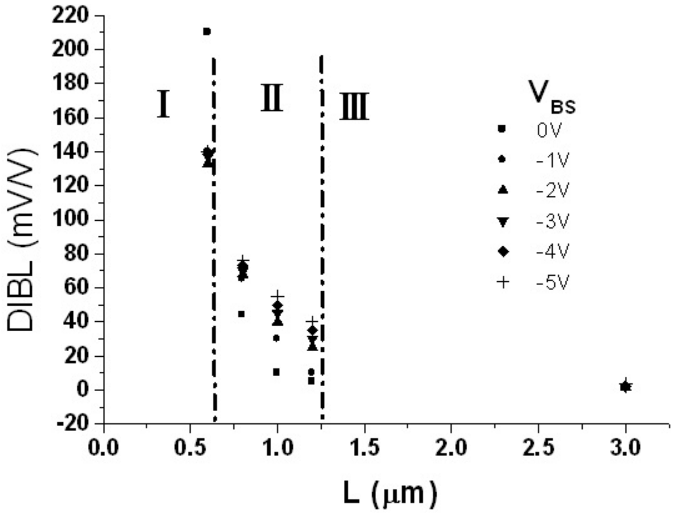

Fig. 3: The measured results of DIBL effect versus channel length L for NMOS devices with V_{BS} varying from 0 to -5 V.

Discussions:

The DIBL effect versus channel length with different substrate voltage bias is infracted divided into the following three regions.

(1)For the short-channel length NMOS in region I($L \le 0.6$ μm) the current is flowing through this subsurface channel at V_{BS} = 0 V as V_{DS} varies from 1 to 5 V. The device is now operating in the punchthrough mode. However, as V_{BS} increases to -5 V, and V_{DS} is 2 V, the device is still operating in punchthrougt mode as shown in Fig. 1(d).In this region, the DIBL versus V_{BS} initially is increased caused by punchthrough effect at zero substrate bias and future decreased as V_{BS} is increased. It's shown that, the minimum design gate length according the process design should not less than the value of 0.6 μm.

(2) For channel length NMOS in region II (0.8 μm <L<1.2 μm) the current flow through the subsurface channel refer as subsurface DIBL.The conduction current will moved from subsurface channel to the surface channel as substrate bias V_{BS} is increased. In this region, the threshold voltage shift d V_{TH} (DIBL) increases as the substrate voltage V_{BS} is increased.

(3) For the long chancel device in region III (L >1.2 μm) the current flow path located on the surface. This is referred on the surface DIBL. This means that most of the conduction current flows along the surface channel, especially for increasing substrate voltage biases. These results also suggest that the DIBL effect in this region would take place mainly along the surface channel, and almost neglected the substrate bias effect for the range of L > 1.2 micron.

Conclusion:

The substrate characteristics of the DIBL effect for short-channel NMOS devices with boron-ion (BF_2^+) channel doping were measured experimentally. The results show that, As the channel length decreases, the threshold voltage shift caused by DIBL first increased with increasing substrate bias and thereafter began decreasing for very short channel devices. This feature could be explained physically by the transition of the surface DIBL effect to the subsurface DIBL effect and the punchthrough effect taking place. The reason for these variations could be explained physically by the change in both the current flow path and the effective channel length of the devices. The substrate bias effect on subthreshold DIBL coefficient (*ETAb*) is approximately 3.5, 7.0, 8.0 and 0.7 mV/V for L of 0.8, 1.0, 1.2 and 3.0 micron respectively. Whereas the subthreshold DIBL coefficient (*ETA0*) is around 44, 10, 5 and 1.25 mV/V respectively. The results present in this paper for the devices of 0.8 micron CMOS technology are well suited to serve as board design guideline for the VLSI device designer. Also our results determined the device performance. Finally, to completely understanding this phenomena, further simulations were carried out by TCAD software with the emphasis on the influence of varying channel length, channel doping, varying junction depth, varying oxide thickness, implantation dose and varying reverse substrate bias on the DIBL have been investigated.

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